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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,334	02/11/2004	Paul Kimelman	550-520	8557

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NIXON & VANDERHYE, PC
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 07/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,334	KIMELMAN ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 11-17* is/are rejected.

7)☒ Claim(s) *7-10 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 23rd of May 2006. Claims 1-11 and 13-20 have been amended; no claim has been canceled; and no claim has been newly added since the Non-Final Office Action was mailed on 23rd of February 2006. Currently, claims 1-20 are pending in this Application.

Response to Amendment

2. The Amendment document in the Response is considered non-compliant because it has failed to meet the requirements of 37 CFR 1.121, as amended on June 30, 2003 (*See 68 Fed. Reg. 38611*, Jun. 30, 2003). In fact, the claim status of the claims 1-11, 13-20 are not using a correct status term (Currently amended), but (Amended). See MPEP 714 [R-3] and 37 CFR 1.121(c). However, the Examiner presumes that the status of the amended claims 1-11, 13-20 are (Currently amended).

Claim Objections

3. Claim 13 is objected to because of the following informalities:

Delete "said" in line 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-5 and 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishimoto et al. [US 5,410,715 A; hereinafter Ishimoto] in view of Cox [US 6,081,867 A].

Referring to claim 1, Ishimoto discloses apparatus for processing data (i.e., microcomputer in Fig. 1), said apparatus comprising:

- processing logic (i.e., CPU 2 of Fig. 1) operable to perform processing operations under control of program instructions (e.g., said CPU processing interrupt service routine) and subject to interruption by a plurality of interrupt events (See col. 1, lines 21-30); and
- a nested interrupt controller (i.e., Interrupt Controller 1 of Fig. 1) operable to control nested execution of a plurality of active interrupt handling programs that are started and uncompleted (i.e., interrupt nesting function) and which is responsive to priorities associated with respective ones of said plurality of interrupt handling programs to control pre-emption of one or more active interrupt handling programs (i.e., interrupt processing under execution) by a pending interrupt handling program (i.e., another interrupt request; See col. 1, lines 31-40); wherein
    - said nested interrupt controller (i.e., said Interrupt Controller) is operable:
        - (i) to permit said pending interrupt handling program (i.e., another new interrupt request) to pre-empt a plurality of active interrupt handling

programs if a priority associated with said pending interrupt handling program is higher than a highest priority associated with any of said plurality of active interrupt programs (i.e., interrupt nesting function; See col. 1, lines 31-40, and col. 7, lines 60-63, and col. 10, lines 25-28); and

- (ii) to prevent said pending interrupt handling program from pre-empting said plurality of active interrupt handling programs if said priority associated with said pending interrupt handling program is less than said highest priority associated with any of said plurality of active interrupt handling programs (See col. 10, lines 23-24).

Ishimoto does not teach that a priority of a given active interrupt handling program is alterable whilst said given active interrupt handling program is started and uncompleted.

Cox discloses a software configurable technique for prioritizing interrupts (See Abstract and col. 2, lines 47-19), wherein

- a priority of a given active interrupt handling program (i.e., a priority of interrupt) is alterable (i.e., changeable; See col. 3, lines 47-52) whilst said given active interrupt handling program is started and uncompleted (i.e., pending interrupt in configuration registers 100 and vector address registers 200 in Figs. 2A-D; See col. 5, lines 53-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said software configurable technique for prioritizing interrupts, as disclosed by Cox, in said nested interrupt controller (i.e., Interrupt Controller), as disclosed by Ishimoto, for the advantage of providing more readily configurable interrupts in comparison to prior techniques (See Cox, col. 1, line 61 through col. 2, line 41, and col. 3, lines 33-35).

Referring to claim 2, Ishimoto teaches

- said nested interrupt controller (i.e., Interrupt Controller 1 of Fig. 1) is operable to prevent said pending interrupt handling program from pre-empting said plurality of active interrupt handling programs (i.e., interrupt processing under execution) if said priority associated with said pending interrupt handling program is equal to a highest priority associated with any of said plurality of active interrupt handling programs (i.e., same priority level; See col. 2, line 65 through col. 3, line 2, wherein in fact that the comparing mean operates to bring the result of comparison into the first level only when the interrupt request generated in the course of execution of the interrupt processing is higher than the priority indicated by the in-service priority information when the information held in the flag is in the first condition clearly implies that said nested interrupt controller is operable to prevent said pending interrupt handling program from pre-empting said plurality of active interrupt handling programs if said priority associated with said pending interrupt handling program is equal to a highest priority associated with any of said plurality of active interrupt handling programs).

Referring to claim 3, Ishimoto teaches

- a priority of an interrupt handling program is set by a programmable priority level associated with said interrupt handling program (See col. 4, lines 60-64).

Referring to claim 4, Ishimoto teaches

- said pending interrupt handling program (i.e., another interrupt request) corresponds to a newly detected interrupt event (See col. 1, lines 31-40).

Referring to claim 5, Ishimoto teaches said nested interrupt controller (i.e., Interrupt Controller 1 of Fig. 1) is responsive to stored values (i.e., interrupting flag in Interrupt Flag 201; and interrupt priority in Interrupt Designation Register 205 in Fig. 2) corresponding to respective ones of a plurality of interrupt events (i.e., Interrupt Requests 3-0...3-7 in Fig. 2) and indicative of:

- a corresponding interrupt handling program being pending or active (i.e., said interrupting flag is set a logic '1', which means "interrupt requesting pending", and reset a logic '0' after receiving Interrupt Processing Acknowledge Signal 21, which means "interrupt requesting active" in Fig. 2; See col. 4, lines 45-48 and col. 5, lines 29-35); and
- a priority level (i.e., interrupt priority (0,0)...(1,1) setting in said Interrupt Designation Register (PR0,PR1)) associated with said corresponding interrupt handling program (See col. 4, lines 48-60).

Referring to claim 12, Ishimoto discloses a method of processing data (i.e., a method of controlling interrupt nesting function; See col. 1, lines 63-67), said method comprising the steps of:

- performing processing operations under control of program instructions (e.g., CPU 2 processing interrupt service routine in Fig. 1), said processing operations being subject to interruption by a plurality of interrupt events (See col. 1, lines 21-30); and
- controlling nested execution of a plurality of active interrupt handling programs that are started and uncompleted (i.e., interrupt nesting function by Interrupt Controller 1 in Fig. 1) and in response to priorities associated with respective ones of said plurality of interrupt handling programs to control pre-emption of one or more active interrupt

handling programs (i.e., interrupt processing under execution) by a pending interrupt event (i.e., another interrupt request; See col. 1, lines 31-40); wherein

- said step of controlling (i.e., interrupt nesting function by said Interrupt Controller) is operable:
  - (i) to permit a pending interrupt handling program (i.e., a new interrupt request) to pre-empt a plurality of active interrupt handling programs if a priority associated with said pending interrupt handling program is higher than a highest priority associated with any of said plurality of active interrupt programs (i.e., interrupt nesting function; See col. 1, lines 31-40, and col. 7, lines 60-63, and col. 10, lines 25-28); and
  - (ii) to prevent said pending interrupt handling program from pre-empting said plurality of active interrupt handling programs if said priority associated with said pending interrupt handling program is less than said highest priority associated with any of said plurality of active interrupt handling programs (See col. 10, lines 23-24).

Ishimoto does not teach that a priority of a given active interrupt handling program is alterable whilst said given active interrupt handling program is started and uncompleted.

Cox discloses a software configurable technique for prioritizing interrupts (See Abstract and col. 2, lines 47-19), wherein

- a priority of a given active interrupt handling program (i.e., a priority of interrupt) is alterable (i.e., changeable; See col. 3, lines 47-52) whilst said given active interrupt handling program is started and uncompleted (i.e., pending interrupt in configuration registers 100 and vector address registers 200 in Figs. 2A-D; See col. 5, lines 53-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said software configurable technique for prioritizing interrupts, as disclosed by Cox, in said step of controlling (i.e., interrupt nesting function by Interrupt Controller), as disclosed by Ishimoto, for the advantage of providing more readily configurable interrupts in comparison to prior techniques (See Cox, col. 1, line 61 through col. 2, line 41, and col. 3, lines 33-35).

Referring to claim 13, Ishimoto teaches said step of controlling (i.e., interrupt nesting function by Interrupt Controller 1 in Fig. 1) is operable to

- prevent said pending interrupt handling program (i.e., a new interrupt request) from pre-empting said plurality of active interrupt handling programs (i.e., interrupt processing under execution) if said priority associated with said pending interrupt handling program is equal to a highest priority associated with any of said plurality of active interrupt handling programs (i.e., same priority level; See col. 2, line 65 through col. 3, line 2, wherein in fact that the comparing mean operates to bring the result of comparison into the first level only when the interrupt request generated in the course of execution of the interrupt processing is higher than the priority indicated by the in-service priority information when the information held in the flag is in the first condition clearly implies that said nested interrupt controller is operable to prevent said pending interrupt handling program from pre-empting said plurality of active interrupt handling programs if said priority associated with said pending interrupt handling program is equal to a highest priority associated with any of said plurality of active interrupt handling programs).

Referring to claim 14, Ishimoto teaches

- a priority of an interrupt handling program is set by a programmable priority level associated with said interrupt handling program (See col. 4, lines 60-64).

Referring to claim 15, Ishimoto teaches

- said pending interrupt handling program (i.e., another interrupt request) corresponds to a newly detected interrupt event (See col. 1, lines 31-40).

Referring to claim 16, Ishimoto teaches said step of controlling (i.e., interrupt nesting function by Interrupt Controller 1 in Fig. 1) is responsive to stored values (i.e., interrupting flag in Interrupt Flag 201, and interrupt priority in Interrupt Designation Register 205 in Fig. 2) corresponding to respective ones of a plurality of interrupt events (i.e., Interrupt Requests 3-0...3-7 in Fig. 2) and indicative of:

- a corresponding interrupt handling program being pending or active (i.e., said interrupting flag is set a logic '1', which means "interrupt requesting pending", and reset a logic '0' after receiving Interrupt Processing Acknowledge Signal 21, which means "interrupt requesting active" in Fig. 2; See col. 4, lines 45-48 and col. 5, lines 29-35); and
- a priority level (i.e., interrupt priority (0,0)...(1,1) setting in said Interrupt Designation Register (PR0,PR1)) associated with said corresponding interrupt handling program (See col. 4, lines 48-60).

7. Claims 6, 11, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishimoto [US 5,410,715 A] in view of Cox [US 6,081,867 A] as applied to claims 1-5 and 12-16 above, and further in view of Hedayat et al. [US 5,642,516 A; hereinafter Hedayat].

Referring to claims 6 and 17, Ishimoto, as modified by Cox, discloses all the limitations of the claims 6 and 17, respectively, except that does not teach stack data storage operable to store state data corresponding to processing pre-empted by one or more active interrupt handling programs.

Hedayat discloses a new interrupt implementation using both hardware and software based interrupt processing (See col. 1, lines 5-8), wherein

- stack data storage (i.e., shadow stack registers SH1-3, SH1a-3a, SH1b-3b, etc. for each data register DR1-3 in Fig. 4; See col. 3, lines 43-45) operable to store state data (i.e., contents of data registers, program counter) corresponding to processing pre-empted by one or more active interrupt handling programs (See col. 4, line 59 through col. 5, line 6).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said stack data storage (i.e., shadow stack registers), as disclosed by Hedayat, in said apparatus (i.e., microcomputer), as disclosed by Ishimoto, for the advantage of providing an optimization of interrupt processing speed through the use of shadow registers hardware processing (See Hedayat, col. 5, lines 6-8).

Referring to claim 11, Hedayat teaches

- said stack data storage (i.e., shadow stack registers SH1-3, SH1a-3a, SH1b-3b, etc. for each data register DR1-3 in Fig. 4) is a stack memory (See col. 3, lines 43-45).

Allowable Subject Matter

8. Claims 7-10 and 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claims 7 and 18, the claim limitations of the respective claims 7 and 18 are deemed allowable over the prior art of record as the prior art fails to teach or suggest that said highest priority level associated with any of said plurality of active interrupt handling programs is increased when free space within said stack data store falls below a predetermined free space level.

The claims 8-10 are dependent claims of the claim 7.

The claims 19-20 are dependent claims of the claim 18.

Response to Arguments

10. Applicants' arguments filed on 23rd of May 2006 have been fully considered but they are not persuasive.

In response to the Applicants' argument with respect to Claims 1-6 and 11-17 rejection under 35 U.S.C. §103(a) for obviousness based on Ishimoto [US 5,410,715] and Cox [US 6,08 1,867] in the Response page 10, line 10 through page 12, line 16, the Examiner respectfully disagrees.

First of all, even though the Examiner admits that pending interrupt priorities are not altered in the primary reference Ishimoto, the secondary reference Cox suggests then claimed limitation, such that a priority of a given active interrupt handling program (i.e., a priority of interrupt) is alterable (i.e., changeable; See Cox, col. 3, lines 47-52) whilst said given active interrupt handling program is started and uncompleted (i.e., pending interrupt in configuration registers 100 and vector address registers 200 in Figs. 2A-D; See Cox, col. 5, lines 53-67). Therefore, the combination of Ishimoto and Cox with rationale for the proper combination suggests the obviousness of the claimed invention.

Secondly, it is noted that the features upon which applicants rely (i.e., interrupts being "trapped" in the system) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Furthermore, as the Applicants refer to Ishimoto's system, it is only necessary for the priority of a new interrupt request to be compared with the currently executing interrupt because pending interrupt requests nested behind the currently executing interrupt are of lower priority by definition, which is suggesting the claimed limitation "... to control pre-emption of **one or more** active interrupt handling programs by a pending interrupt handling program..." in the exemplary claim 1. In other words, the scope of the claimed invention is within the Ishimoto's system with the exception of the Examiner's admittance "pending interrupt (actually, active interrupt handling program) priorities are not altered in the primary reference Ishimoto," such that the priority of a pending interrupt handling program (i.e., new interrupt request) is compared with the one (i.e., one or more) active interrupt handling program (i.e., currently executing interrupt).

Thirdly, even though the Applicants argue that Cox does not provide any teaching with regard to nesting interrupt requests, the primary reference Ishimoto clearly anticipates the teaching with regard to nesting interrupt requests.

Moreover, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Finally, it is noted that the features upon which applicants rely (i.e., making a new interrupt, viz., a pending interrupt handling program, compare with the other nested interrupts, viz. multiple active interrupt handling programs) are not recited in the rejected claim(s). Although

the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Thus, the Applicants' argument on this point is not persuasive.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christopher E. Lee
Patent Examiner
Art Unit 2112

CEL/